

Final Report  
For NASA Contract  
NAS8-26379

August 1977

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This final report is a representative condensation of the work done under NASA Contract NAS8-26379 during the period September 1, 1974 through December 31, 1976. This work has had three primary objectives:

- 1) The further development and improvement of a novel high speed x-ray topographic camera to be used in semiconductor process control.
- 2) the study of the effects of process-induced defects identified by the camera on the performance of some semiconductor devices.
- 3) the support of application of the new camera to current industrial process control problems.

Section II of this report gives a very brief introduction to the application of x-ray topography to semiconductor process control, a description of the novel features of the high speed camera, and a discussion of the technical difficulties associated with the practical implementation of this technique.

Our most significant results on the effects of material defects on device performance are included in Section III. These results were obtained using wafers processed entirely within the Institute for Solid State Electronics. Defects were identified using the x-ray camera and correlations made with probe data. Also included are temperature dependent effects of material defect

Section IV is a summary of application and recent improvements including x-ray topographs of silicon-on-sapphire and gallium arsenide. A description of a real time TV system prototype and of the most recent vacuum chuck design is given. Discussion is included of our promotion of the use of the camera by various semiconductor manufacturers. The final section contains the conclusion.

## II. THE HIGH SPEED X-RAY TOPOGRAPHIC CAMERA

For many years it has been known that strained regions of an otherwise perfect crystalline lattice produce contrasts in the diffracted x-ray image. The strains may be caused by substituted atom mismatch, point defects, dislocations, or film interface stress. The importance of crystalline quality has been recognized since the beginning of semiconductor device technology and x-ray topography has been used to monitor the crystalline perfection. The nondestructive nature of the technique is particularly useful in identifying process induced defects since the same specimen may be examined after each of the several typical thermal cycles used in most fabrication processes.

The condition for x-ray diffraction requires that a beam of parallel, monochromatic x-rays strike a selected set of crystalline planes at a specific critical angle called the Bragg angle. Since practical lens or mirrors for x-rays do not, as yet, exist the incident parallel beam is achieved in practice by using a distant point source of x-rays (i.e. the electron focal spot of an x-ray tube). The x-ray spectra is sufficiently rich in the anode material characteristic wavelength to be effectively monochromatic. If the crystalline planes are flat only those rays on a conical surface whose vertex angle is the complement of the Bragg angle can satisfy the condition for x-ray diffraction. Conventional x-ray topographic cameras use a small portion of the rays in this cone (the rays in the cone that intercept the specimen) to form the diffracted image. Large segments of the specimen can only be imaged by a scanning mechanism which moves the wafer and film. This is a very slow inefficient process since only a narrow section of the specimen wafer is being imaged at any one time.

The new high speed camera, developed under this contract, is identical with the conventional reflection topographic camera (Berg-Barrett) with the single exception that the wafer is elastically deformed such that all the rays diverging from the point source that strike the wafer strike it at the Bragg angle. This allows the image of the entire wafer to be formed in the same time that a single narrow strip can be formed by the conventional techniques. The exposure time is reduced by at least one order of magnitude.

The desired shape of the deformed wafer closely approximates a sphere. The radius of bending depends on the wavelength of the radiation used, the atomic lattice planes used for the particular diffraction, and the orientation of the wafer. Typical radii of curvature are 100 to 200 inches, thus the total deformation is very small. The diagram in figure 1 shows the geometrical relationship of the camera parts.

The ultimate resolution limit of the new camera is the same as the Berg-Barrett which depends on the x-ray tube focal spot size, source-to-wafer distance, wafer-to-film distance, the wavelength spread of the particular x-ray tube target radiation, the lattice planes used for the diffraction, and/or the film type. When Kodak high resolution plates are used the geometrical relations for a typical camera configuration limit the resolution in the 10 micron range.

Several techniques have been used to bend the wafer to the desired shape. One method is to use spherically curved vacuum chuck with multiple vacuum feed points. Since this fixes the curvature a different chuck must be custom made for each camera configuration to be used (i.e. wafer material, diffracting planes used, wafer orientation, and x-ray tube wavelength). Small deliberate or accidental misorientations of the wafer cut make this method undesirable unless the material orientation is controlled. Also

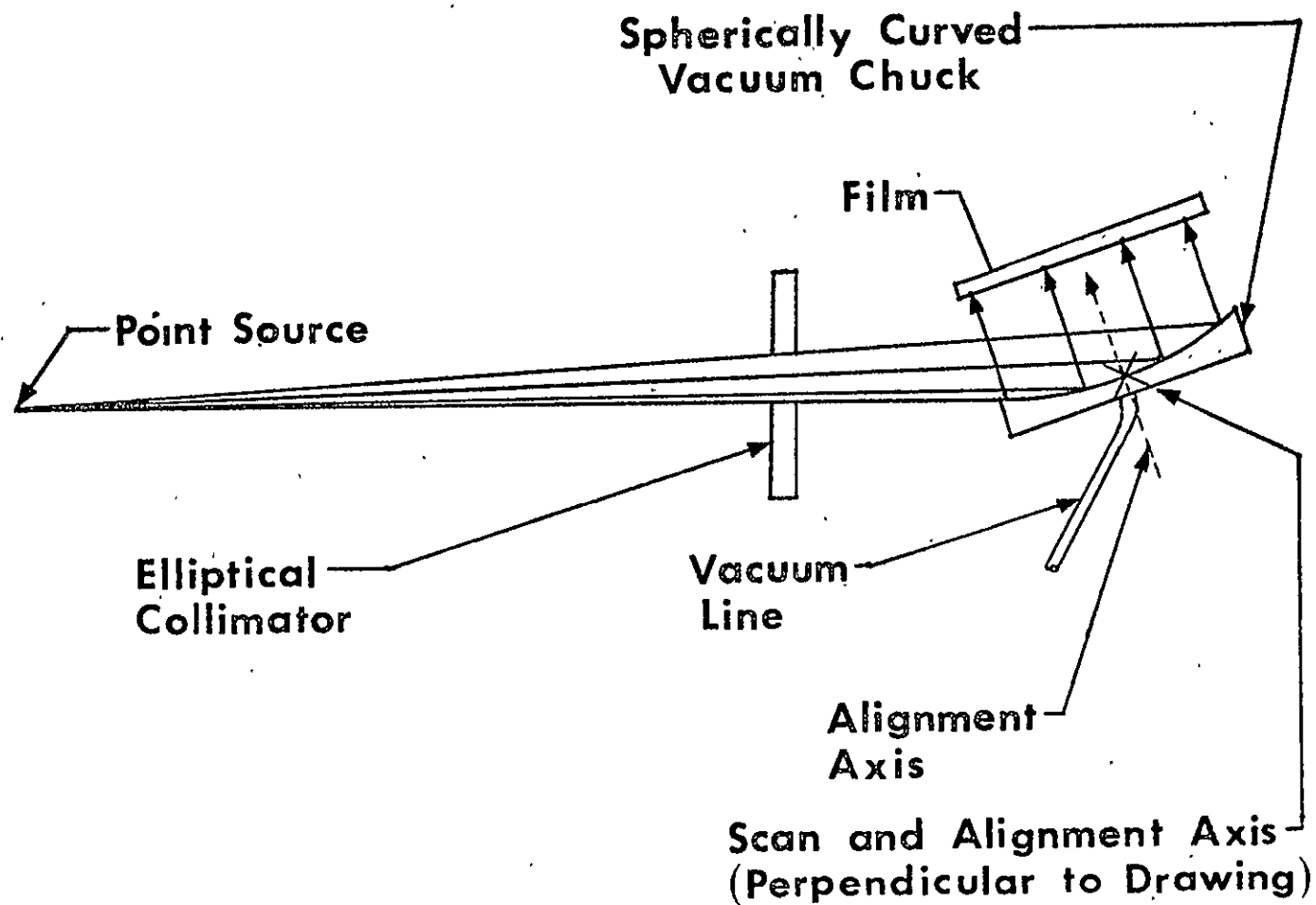


Figure 1

the differential pressure used to deform the wafer must be limited to the minimum required to force the wafer to conform to the chuck shape. A total vacuum will produce high stress points at the vacuum feed holes which appear in the topographs as dimples. A universal elastic chuck which overcomes these difficulties is described in Section IV.

Random bending errors always prevent the imaging of an entire wafer with a single fixed setting of the camera. The percentage of total area varies greatly with the amount of processing damage. The minimum area is about 50% for severely warped wafers and ranges up to about 95% for typical two inch wafers which have been completely processed. The difficulties encountered with warped wafers is common to all types of x-ray topography and can be avoided by slightly rocking the wafer during the x-ray exposure. This does lower the resolution and increase exposure time somewhat.

In summary, the novel feature of the new high speed camera results in a substantial savings in cost-per-topograph. This savings allows reconsideration of the technique for direct process control.



### III. DEFECT-PROBE CORRELATION

#### A. Temperature Dependence of Reverse Bias Characteristics in Dislocated Diodes

This section presents the details of the diode fabrication, dislocation generation and diode testing. Care was taken to keep the experiment simple, meeting all the necessary experimental conditions with a minimum number of variables. Sufficient testing on the devices was done so that the results are directly applicable to commercially fabricated devices.

#### DEVICE PREPARATION

##### Mask Preparation:

A special mask set was made to minimize surface effects in the reverse bias characteristics. This technique is used by many researchers to study bulk junction effects and consists of a diffused guard ring of the same impurity species and the diode under study. The impurity concentration and junction depth of each of two overlapping diffusions (diode and guard ring) are such that the diode should breakdown first under reverse bias.

Scale replicas of the mask set are shown in Figs. 2-5. The first diffusion pattern forms the guard ring and a resistor for monitoring uniformity. The second diffusion pattern forms the planar junction under study and another resistor. The contact and metallization pattern complete the set with the additional features of

1. front side access to the substrate
2. an insulated gate on the diode and
3. the MOS capacitor (not used for this experiment).

The size of the bar is 50 x 50 mils with the diameter of the planar portion of the diode about 18 mils (portion of the second diffusion that does not overlap the first). Actually, only one mask was made with all four

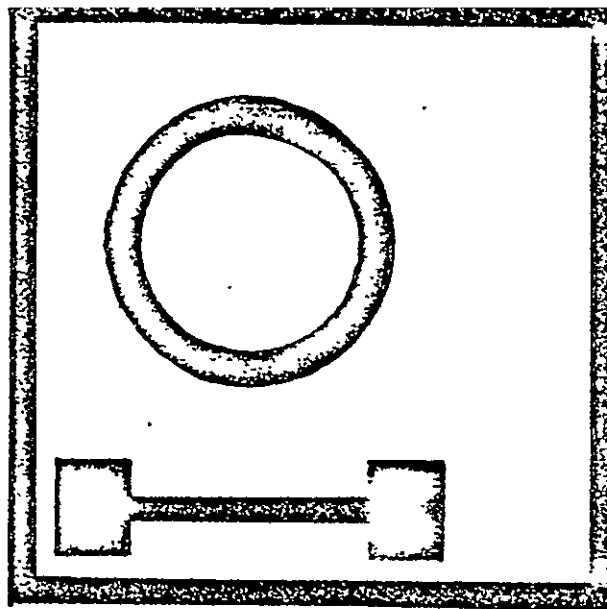


Figure 2 First diffusion pattern.

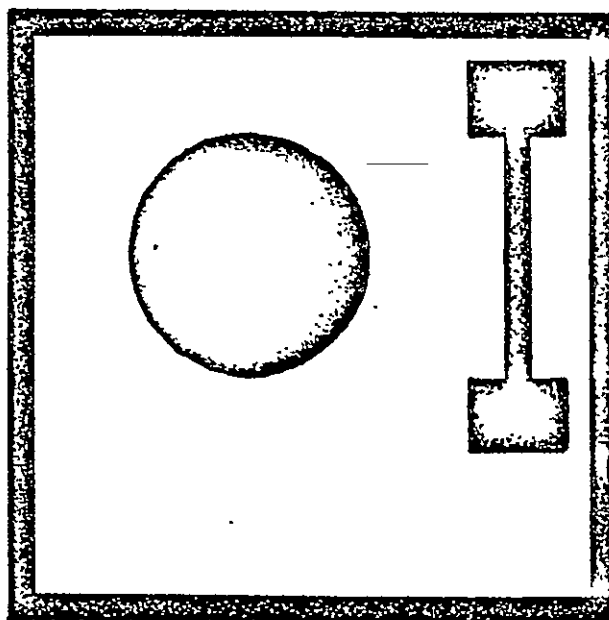


Figure 3 Second diffusion pattern.

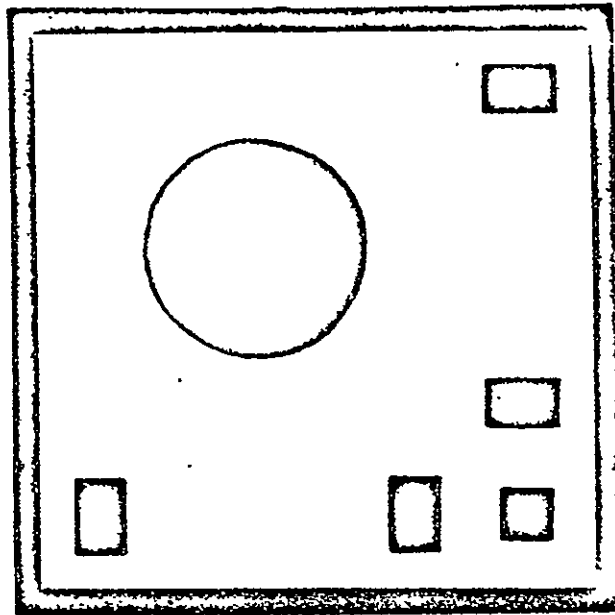


Figure 4 Contact pattern.

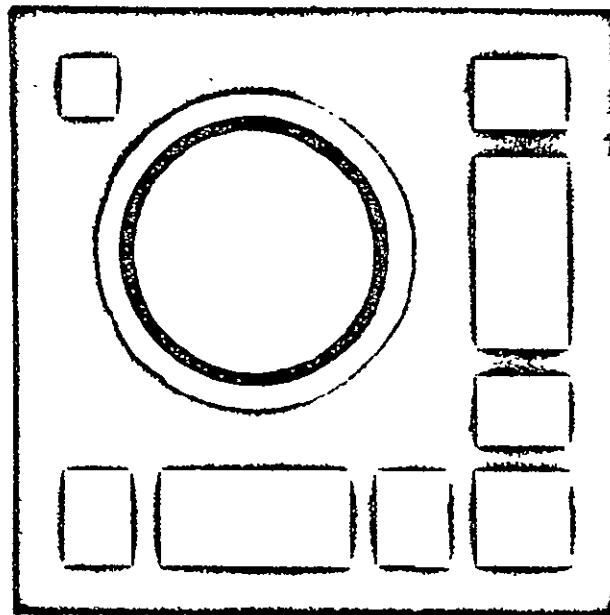


Figure 5 Metallization pattern.

patterns in a 100 x 100 mils square array. During the second, third and fourth photolithographic steps the mask is shifted over and/or down 50 mils with respect to the first step. This procedure eliminates 3/4 of the wafer material but still provides a more than adequate number of diodes per wafer for experimental purposes. The first reduction was 33 1/3 x with a 3x reduction during the step and repeat exposure.

#### Fabrication:

The basic processing steps for the diffused devices are outlined in Table I. During the deposition cycle the wafers were processed in the "flat" position on a quartz boat to obtain uniform impurity deposition. A liquid source,  $\text{BBr}_3$ , was used as the dopant.

#### Dislocation Generation:

Anomalous stress and dislocations usually appear after an oxidation, diffusion, or a drive-in cycle. Thermal oxidation may introduce dislocations because of the mismatch of the thermal expansion coefficient of silicon and silicon dioxide. However, little attention has been given to the selective creation of defects as it is necessary to maintain maximum control over experimental conditions.

In this work the dislocation generation step was performed after the first oxidation and consisted of a rapid thermal cycle to 1150° with the wafer lying horizontally over the hole as mentioned above or, in some cases, the wafer lying horizontally with the edges overhanging the quartz boat. Whether a diode has defects or not was ascertained by careful examination of the original X-ray negative and for correlation the defects must appear inside the diode.

TABLE I Diffused device process

Starting material - N21, N22, <111> 2" diameter, Silicon  
N - type (phosphorous), 2 - 4 ohm-cm.  
EPC - less than  $10^3 \text{ cm}^{-2}$

Processing Steps :

1. Oxide growth (steam)  
Temp 1000°C 5500A°  
Temp 1150°C Defect generation
2. 1<sup>st</sup> diffusion (boron liquid source)  
(a) Deposition 900°C, ( $C_s = 5 \cdot 10^{19} \text{ at/cm}^3$ )  
(b) Drive-in 1150°C, Resistivity -  $160 \Omega/\square$   
Junction depth =  $4 \mu$
3. 2<sup>nd</sup> diffusion (boron liquid source)  
(a) Deposition 900°C, 15 min.  
Resistivity =  $152 \Omega/\square$   
(b) Drive-in 1100°C  
Resistivity =  $340 \Omega/\square$   
Junction depth =  $1.6 \mu$
4. Metallization (aluminum)  
Thickness =  $1 \mu$   
Annealing at 495°C 15 min.

## Electrical Measurements

Electrical measurements were conducted on wafers soon after the annealing step to avoid any possible changes on the surface that could occur if the devices were left exposed to atmospheric conditions for an extended period of time. The reverse I-V characteristics were studied by probing the diffused diodes on the entire wafers N21 and N22. Photoelectric effects were minimized by conducting measurements in the dark.

## TEMPERATURE DEPENDENCE MEASUREMENTS

### Device Evaluation

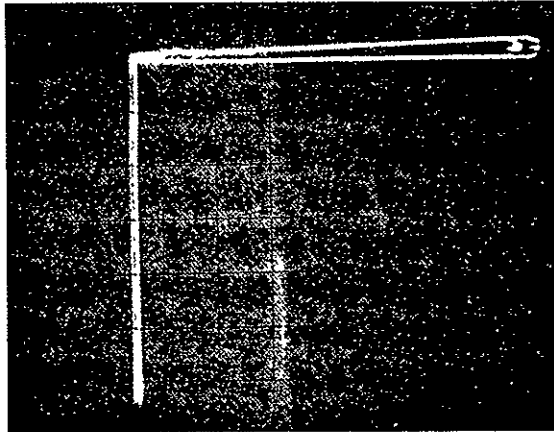
To study the reverse characteristics in detail, the diodes were classified in several groups described below.

For reverse leakage current measurement, diodes are classified in three categories.

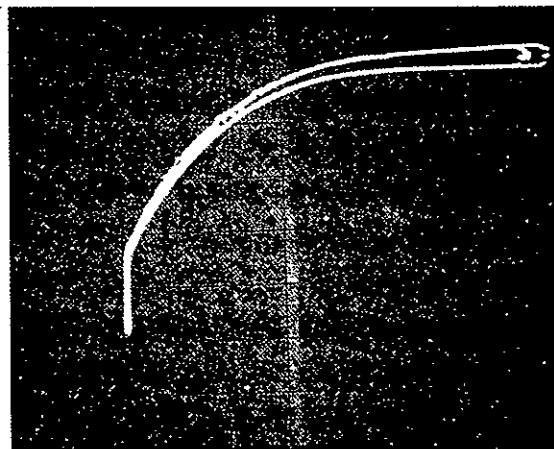
- |           |  |
|-----------|--|
| Class-I   | Reasonably hard diodes <u>which</u> have reverse leakage current less than 20 nanoamperes at the breakdown voltage.  |
| Class-II  | Medium soft diodes in which the sharp breakdown exists but the reverse leakage current at breakdown is in the microamperes range.                                  |
| Class-III | Soft diodes in which the breakdown voltage is difficult to define and which have more than 20 microamperes reverse leakage current at about 65 volts reverse bias. |

Typical characteristics of all three classes are shown in Figs. 6a, 6b, and 6c respectively.

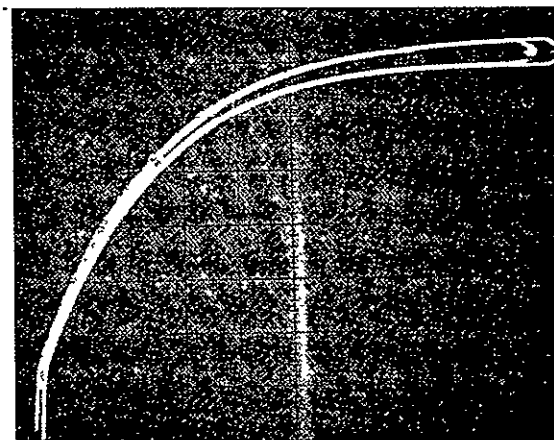
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(a)



(b)



(c)

Figure 6 Typical I-V characteristics of a  
(a) hard diode (b) medium soft diode  
and (c) soft diode.

For avalanche breakdown measurements a total of sixteen diodes from Class-I and Class-II were chosen. In each class the diodes have a sharp breakdown. A change in the reverse bias of a few millivolts results in three to four decades of change in the reverse current. Among these, eight diodes have 75 volts breakdown voltage and four diodes have 78 volts breakdown voltage. The remaining four diodes have 60 volts, 73 volts, 62 volts, and 84 volts breakdown voltage.

Each of these diodes were separated from the array by 'dicing' and were mounted in a 3 pin TO 5 header. Thermocompression bonding was used to bond gold wires from the diode to the pins. Each diode was checked to see whether it had defects or not by examining the X-ray topograph. This was done before mounting the diode on the header.

An insulated box was constructed for measuring the thermally stimulated current and avalanche breakdown voltage of the  $P^+-N$  junction. The apparatus was designed to facilitate the electrical characterization of the  $P^+-N$  junction diode mounted in a three pin TO 5 header (as described earlier). The temperature of the diode was measured with a copper-constantan thermocouple attached to the TO 5 header near the silicon chip. The temperature measurement accuracy was in the range of  $\pm 2^\circ K$ .

After mounting the TO 5 header inside the insulated box, the box was heated to  $40^\circ C$  during a dry nitrogen gas purge for at least ten minutes to remove the moisture. This was necessary to avoid any surface problems such as icing. The insulated box was then cooled down to about  $120^\circ K$  by introducing liquid nitrogen. A fan was kept running continuously to circulate the gas inside to eliminate any temperature gradient that might otherwise exist. The temperature was raised gradually with a heater inside the box. The heating rate was gradual, requiring about three hours



to raise the temperature to 400°K. This process was considered isothermal.

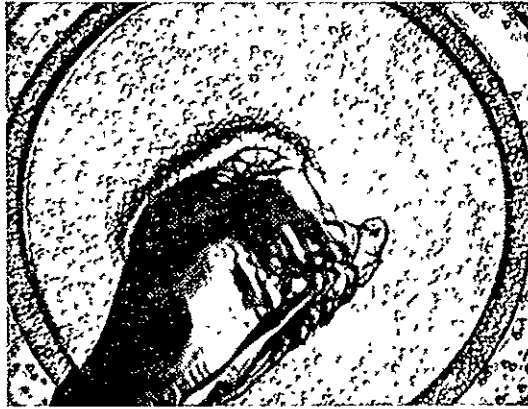
To minimize measurement inaccuracies, considerable time was spent on optimizing the wiring of different pieces of the test equipment to eliminate noise and ground problems which are particularly important with low level measurements.

Reverse leakage current measurements were conducted by supplying 30 volts reverse bias to the diode. Avalanche breakdown voltage data were taken supplying constant current through the diode. The accuracy in breakdown measurements was  $\pm 0.5$  volts. These measurements were by far the most time consuming, since they had to be evaluated every two or three degrees to see any noticeable change. The temperature and characteristics were simultaneously noted and then the temperature was raised (by heating) about two or three degrees. The next measurement was taken after the temperature inside the box stabilized (after at least two minutes).

After taking the measurements, all diodes were subjected to Sirtl etch for four minute. The dislocations were counted individually for each diode. The diodes have either none, scattered, or lineage type defects and typical examples of each are shown in Fig. 7.

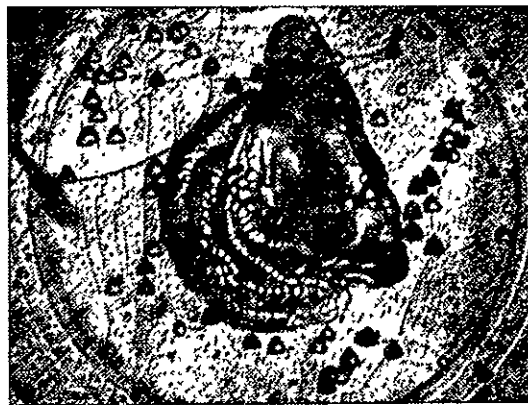
#### Experimental Results

The reverse leakage current, (30 volts reverse bias) for the temperature range 120°K to 400°K, for groups of P-N diodes is shown in Figs. (8,9 & 10). It appears that in Class I diodes the reverse leakage current varied from  $10^{-11}$  to  $10^{-5}$  amp. In Class II diodes it varied from  $10^{-9}$  to  $10^{-5}$  amp. In Class III diodes it varied from  $10^{-7}$  to  $10^{-5}$  amp. The type of dislocations and density of these dislocations for each diode are summerized in Table II.

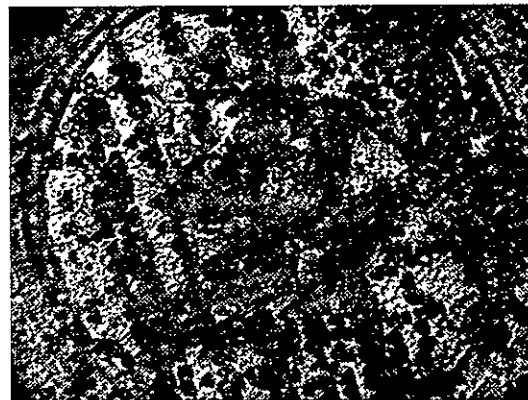


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(a)



(b)



(c)

Figure 7 (a) Diode without defects,  
(b) diode with scattered defects and  
(c) diode with lineage type defects.

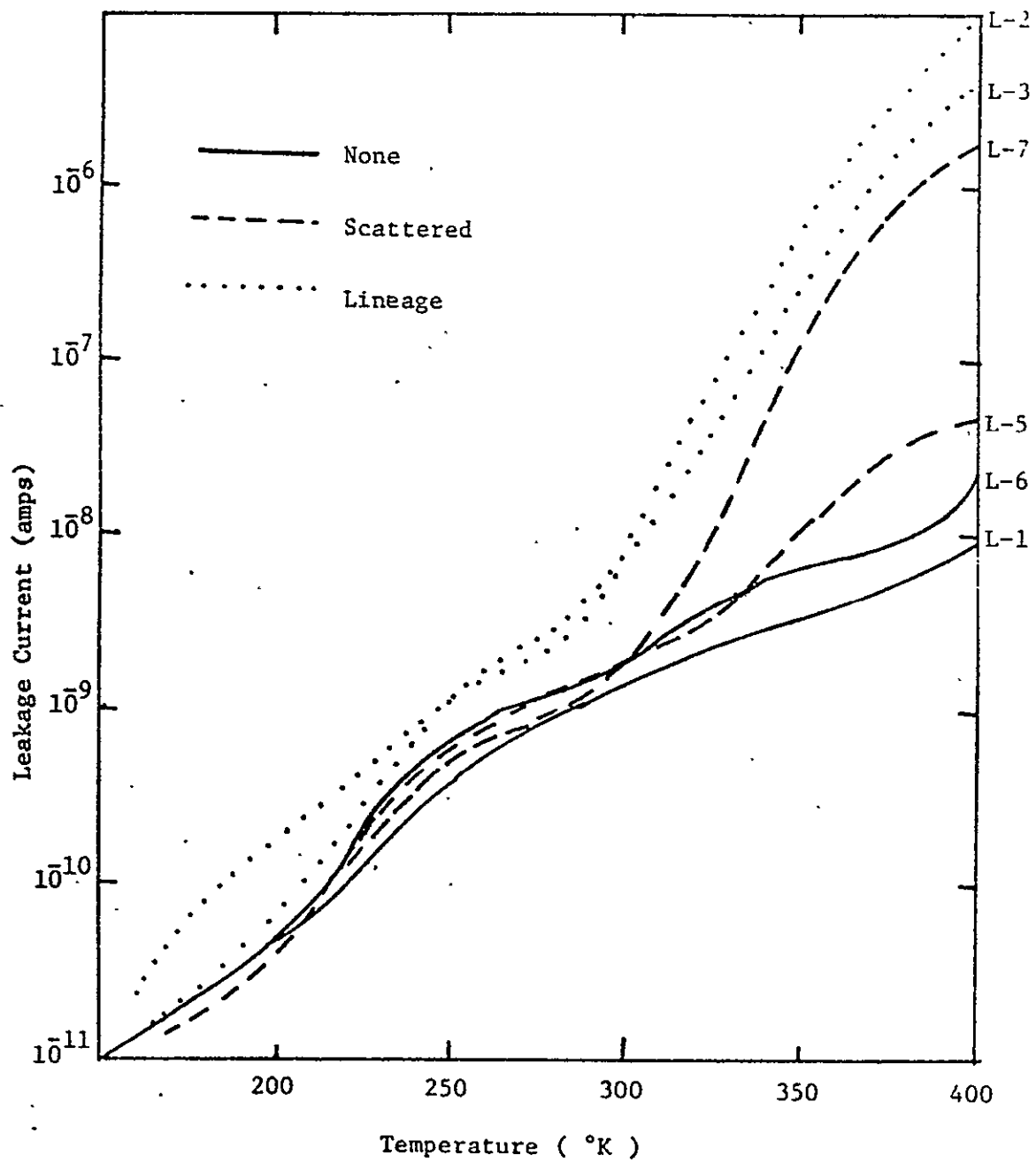


Figure 8 Class I diodes

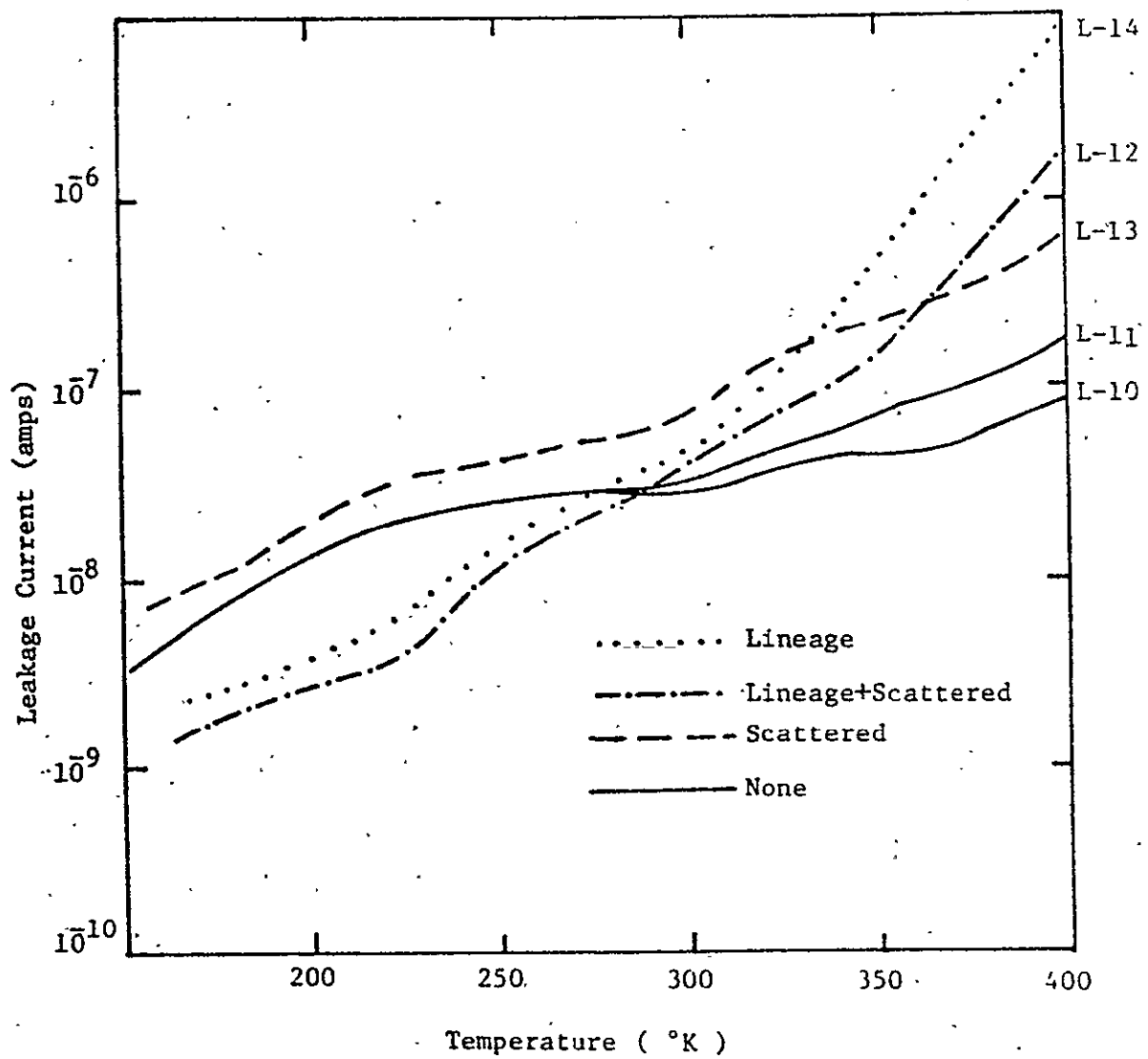


Figure 9 Class II diodes

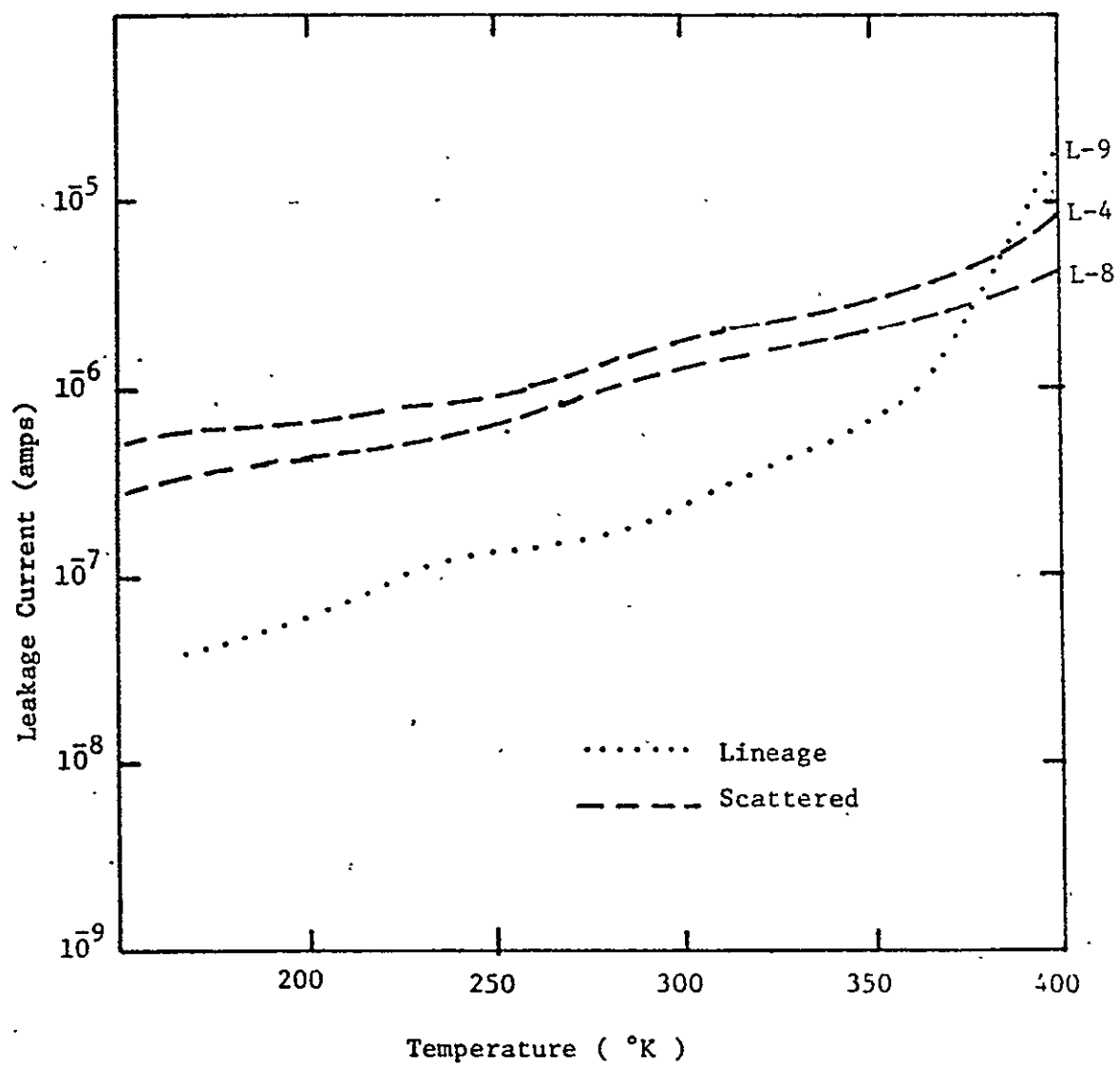


Figure 10 Class III diodes

TABLE II: DISLOCATIONS IN DIODES

Diodes	Feature of Dislocations	Dis. density ( $\text{cm}^{-2}$ )
L-1	Scattered	$2 \times 10^3$
L-2	Lineages	$1.4 \times 10^6$
L-3	Lineages	$1.35 \times 10^5$
L-4	Scattered	$5.5 \times 10^4$
L-5	Scattered	$3.0 \times 10^3$
L-6	None	None
L-7	Scattered	$6.5 \times 10^4$
L-8	Scattered	$1.0 \times 10^4$
L-9	Lineages	$1.2 \times 10^6$
L-10	None	None
L-11	None	None
L-12	Lin + Scatt.	$3.0 \times 10^5$
L-13	Scattered	$1.0 \times 10^3$
L-14	Lineages	$5.0 \times 10^5$
L-15	Scattered	$5.0 \times 10^4$
L-16	Scattered	$1.0 \times 10^4$

The breakdown voltages of several diodes were measured for the temperature range 120°K to 400°K. Typical results are shown in Fig. 11. The type of dislocacations, density of dislocations, change in breakdown voltage and leakage current (at room temperature) at the breakdown point for each diode are presented in Table III. A noticeable feature regarding the characteristic is that the soft characteristic has a tendency to become hard at low temperatures and the hard ones become soft at high temperatures. Secondly, it should be noticed that the diodes possess a positive temperature coefficient.

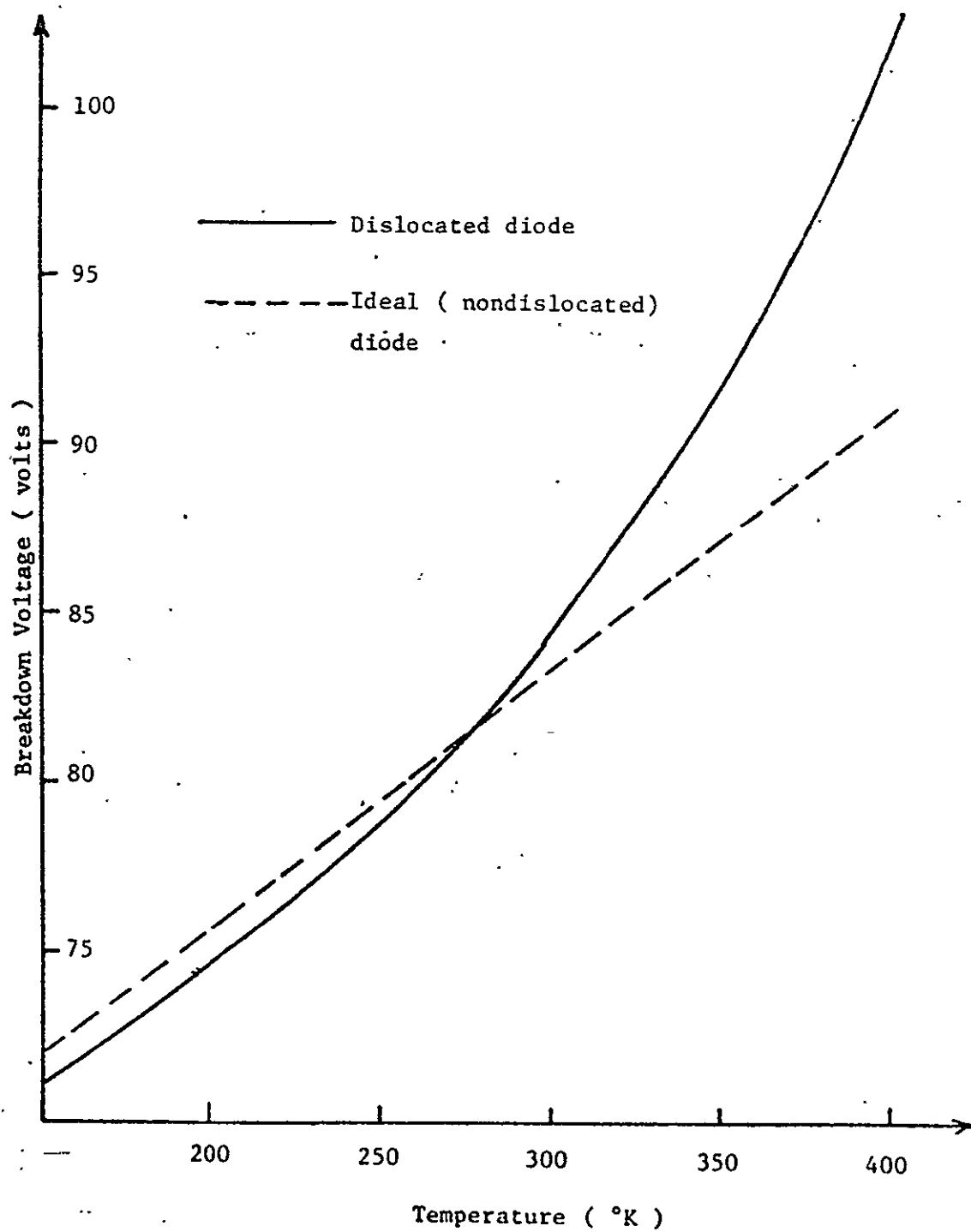


Figure 11 Typical breakdown voltage curves



TABLE III BREAKDOWN VOLTAGE

DIODE	Breakdown Voltage at room temp.	Measured Breakdown Voltage 121°K-400°K (Volts)	Experimental total change in BV (Volts)	Ideal theoretical* total change in B.V. (Volts)	Dislocation Density (cm <sup>-2</sup> )	Feature of dislocation†
B-1	60	50-70.3	20.3	14.8	$3 \times 10^5$	L
B-2	62	53.1-72.1	19.0	15.3	$3.6 \times 10^5$	S
B-3	73	61-88	27.0	17.8	$2 \times 10^3$	S
B-4	75	64-84.6	20.6	18.5	NONE	-
B-5	75	63-85	22.0	18.5	NONE	-
B-6	75	62.9-86	23.1	18.5	$1 \times 10^3$	S
B-7	75	62.8-92.7	29.7	18.5	$2 \times 10^4$	S
B-8	75	65.8-101	35.2	18.5	$3 \times 10^4$	L
B-9	75	64-84.2	20.2	18.5	NONE	-
B-10	75	64-104	40.0	18.5	$8 \times 10^5$	L
B-11	78	66.9-86.4	19.5	19.22	NONE	-
B-12	78	64-95.1	31.1	19.22	$6 \times 10^4$	S
B-13	78	63-92.3	29.3	19.22	$8 \times 10^4$	S
B-14	78	63.1-101	37.9	19.22	$1 \times 10^5$	L
B-15	78	62.8-102	39.2	19.22	$4 \times 10^5$	L
B-16	84	68-103	35.0	20.7	$1.2 \times 10^6$	L

\* Using McKay theory (22)

† S-Scattered L-Lineages

## B. Reverse Leakage and Breakdown at Room Temperature

The probe correlation study was done on wafers (N21 and N22). These two wafers were processed simultaneously except for the abrupt thermal cycle to produce the lattice defects. Four wafer facsimiles are shown in Fig. 3.1a-3.1d which display the distribution of diodes with observable defects superimposed with the distribution of diodes which failed leakage current and reverse bias breakdown probe tests.

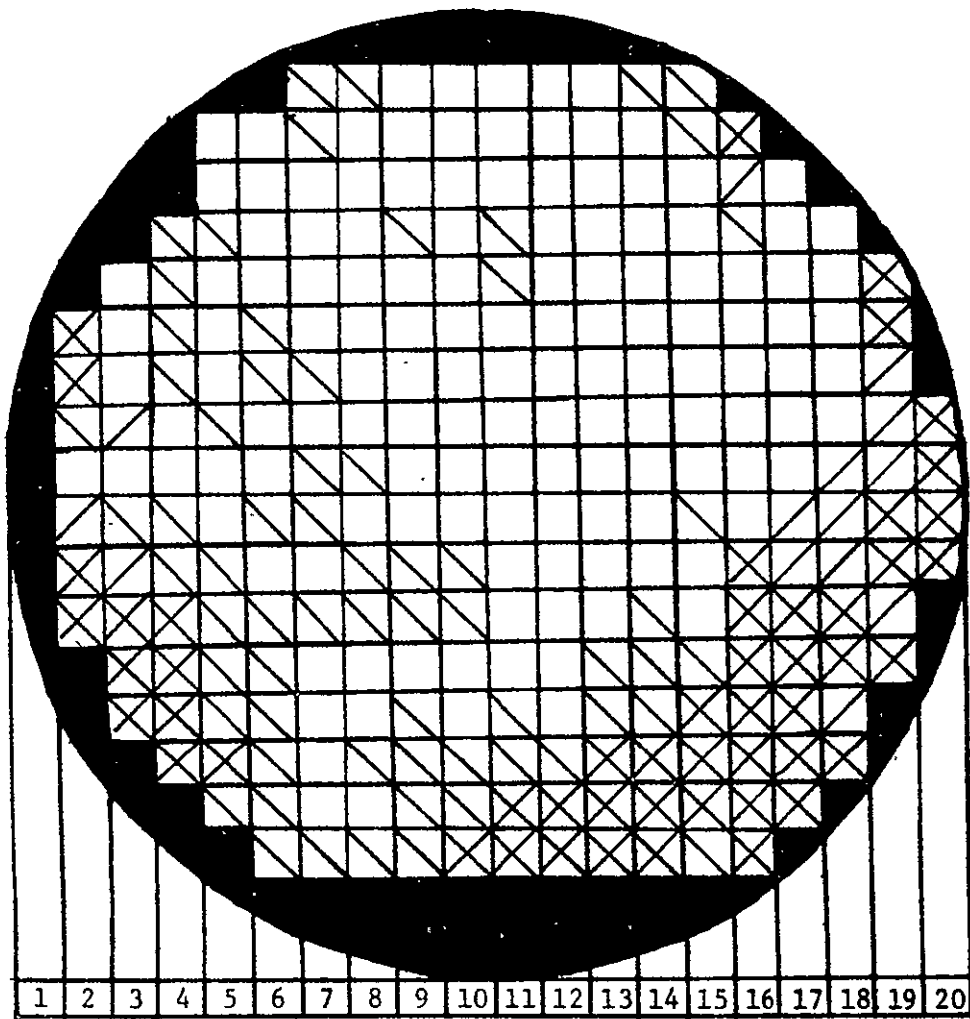
### Analysis and Discussion:

Thermally induced defects were created purposely in virtually dislocation free (less than  $10^3 \text{ cm}^{-2}$ ) crystals after the oxidation step to get overall control on the experimental conditions. The purpose of the X-ray topograph is to obtain information on the crystal imperfection non-destructively. In the probe correlation study, an attempt was made to correlate the electrical characteristics with the imperfection information contained in the X-ray topographs. For reverse leakage current and avalanche breakdown, the probe testing results were divided into the following categories.

- (1) Diodes with reverse leakage current less than 5 microamperes considered to pass the test. It is assumed that this range will take care of any effects on reverse leakage current due to metal precipitations or any surface contamination.
- (2) Diodes with leakage current greater than or equal to 5 microamperes are considered to fail the test. This large current is due to defects in the diodes.
- (3) Diodes with breakdown voltages greater than 50 volts considered to pass the test. The curvature of the junction is slightly different from diode to diode, which results in fluctuations

Wafer N21

Test Leakage current  $\geq 5 \mu\text{a}$



☐ - Indicates device failed probe test

☒ - Indicates defects shown in X-ray topograph

% Good Devices 57 %

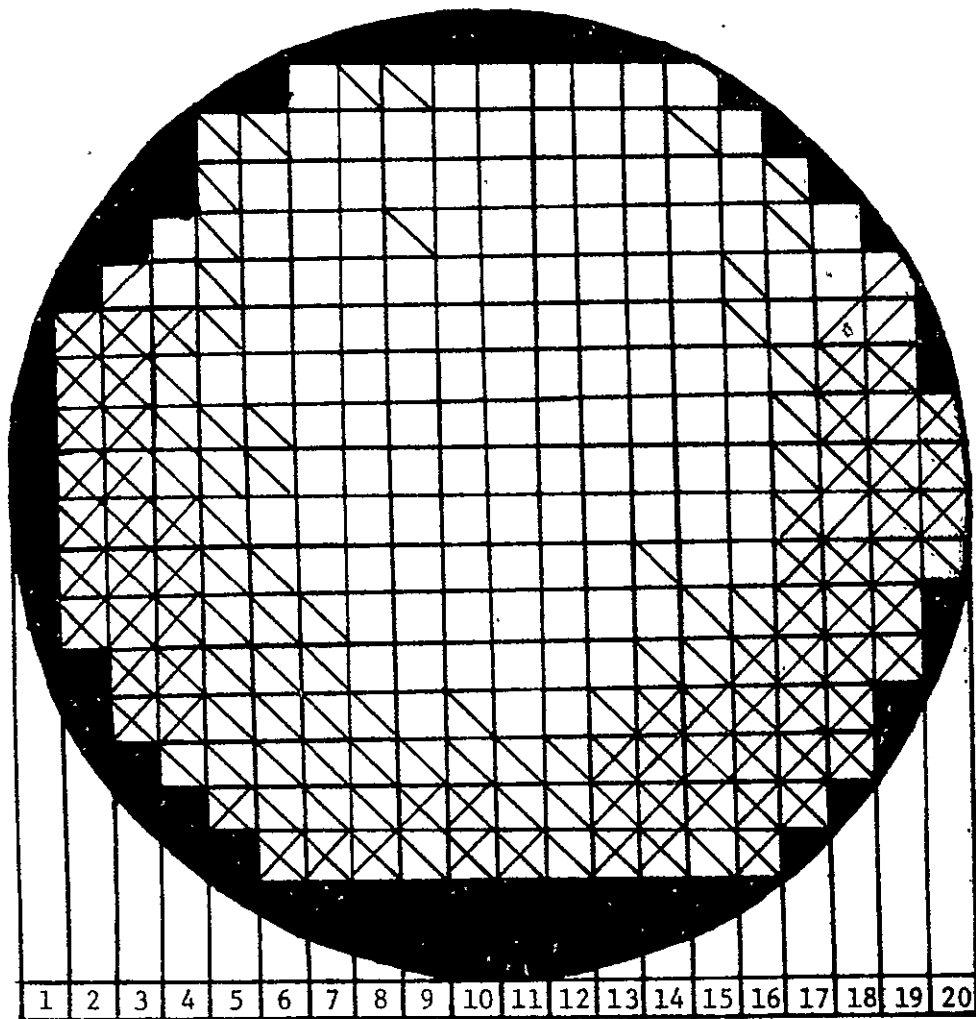
% Correlation 70 %

Figure 3.1 a

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Wafer N22

Test Leakage Current > 5  $\mu$ a



☐ - Indicates device failed probe test

☒ - Indicates defects shown in X-ray topograph

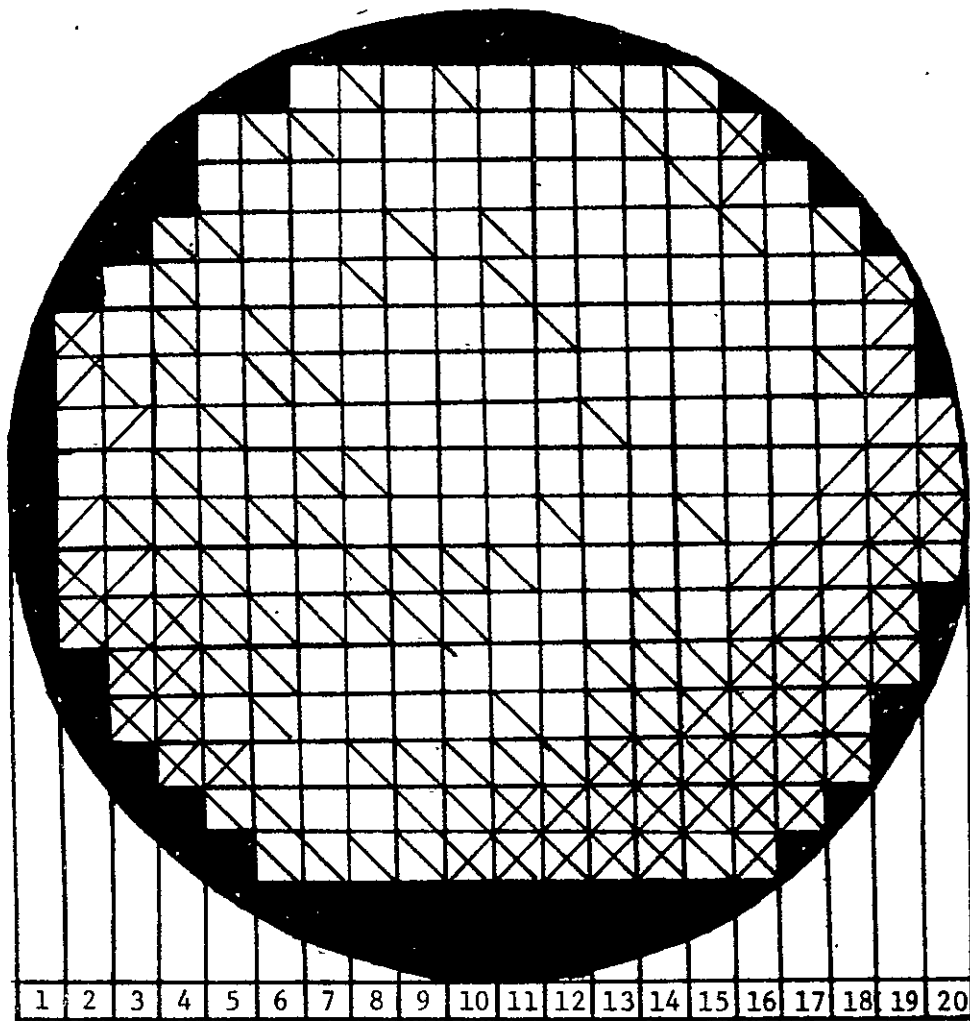
% Good Devices 50.5 %

% Correlation 74.5 %

Figure 3.1 b

Wafer N21

Test Breakdown < 50 volts



☐ - Indicates device failed probe test

☑ - Indicates defects shown in X-ray topograph

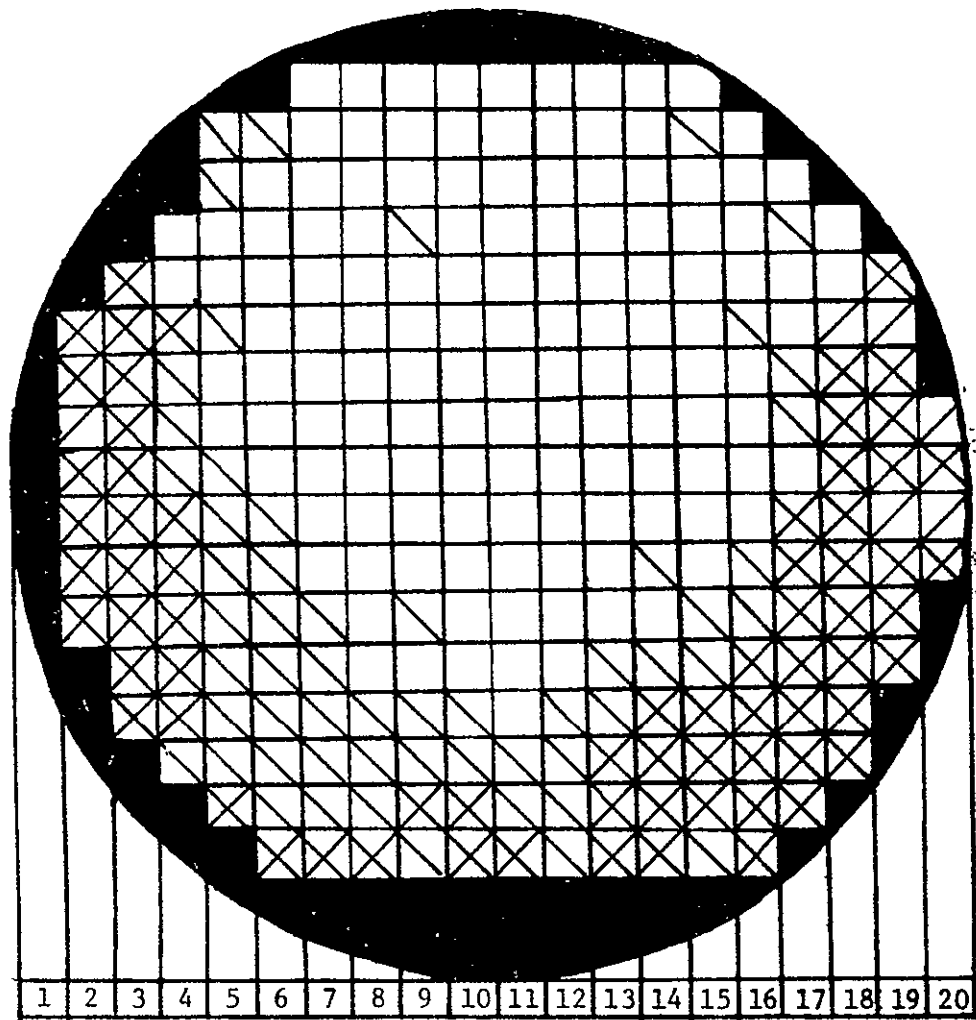
% Good Devices 55.5 %

% Correlation 66 %

Figure 3.1 c

Wafer N22

Test Breakdown < 50 volts



☐ - Indicates device failed probe test

☒ - Indicates defects shown in X-ray topograph

% Good Devices 52.5 %

% Correlation 76.5 %

Figure 3.1 d

in the breakdown voltage.

- (4) Diodes with avalanche breakdown less than or equal to 50 volts are considered to fail the probe test.

A correlation summary for each wafer which gives a column by column count of the number of diodes in each of the above four categories are presented in Tables IV -- VII. The percentage correlation is calculated as follows.

$$\% \text{ Correlation} = 100 \times \frac{\left| \begin{array}{l} \text{The number of diodes} \\ \text{that passed probe test} \\ \text{and show no defects in} \\ \text{the X-ray topograph} \end{array} \right| + \left| \begin{array}{l} \text{The number of diodes} \\ \text{that failed probe test} \\ \text{and show defects in} \\ \text{the X-ray topograph} \end{array} \right|}{\text{TOTAL NUMBER OF DIODES}}$$

The average correlation for both wafers for both probe tests (reverse leakage current and avalanche breakdown) is about 72%. A significant number of diodes failed probe tests and yet had no defects visible in the x-ray topographs. Random Sirtl etching of these diodes indicate that they have a few isolated dislocations which may contribute to their failure. The following conclusions can be drawn from the correlation study. Diodes in the undamaged area yielded 90% to 95% reasonable hard; whereas, those diodes in the area heavily dislocated yielded about 10% to 20% hard. The dislocations ( $> 10^4 \text{ cm}^{-2}$ ) which significantly degrade the hardness of the diode's reverse characteristics are most probably due to (a) dislocations providing a path for channel injected minority carries through the P-N junction's depletion region or (b) the dislocations are creating current by the generation-recombination process.

Table IV Correlation SummaryWafer N21Device Diode with Guard RingTest Leakage Current > 5ua

Device Evaluation Probe	Material Characteri- zation by X-ray	C O L U M N																				Category Total
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Passed	Good Material	0	1	4	2	7	7	10	11	10	12	11	14	12	10	9	6	7	5	0	0	138
Failed	Defects	0	4	3	4	1	0	0	0	0	1	2	2	3	3	3	8	4	3	5	3	49
Passed	Defects	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	2	4	4	1	14
Failed	Good Material	0	1	2	6	7	9	7	6	7	4	4	1	2	4	5	1	1	0	0	0	67
Column Total		0	7	10	12	15	16	17	17	17	17	17	17	17	17	17	16	14	12	9	4	268

% Good Devices 57%% Correlation 70%



Table V Correlation SummaryWafer N22Device Diode with Guard RingTest Leakage Current > 5ua

Device Evaluation Probe	Material Characteri- zation by X-ray	C O L U M N																				Category Total
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Passed	Good Material	0	0	0	2	1	5	11	12	12	13	14	14	13	11	10	7	2	2	0	0	129
Failed	Defects	0	7	9	6	1	1	1	1	1	2	1	0	3	4	3	5	7	8	6	4	70
Passed	Defects	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	3	0	6
Failed	Good Material	0	0	0	4	13	10	5	4	4	2	2	3	1	2	4	4	5	0	0	0	63
Column Total		0	7	10	12	15	16	17	17	17	17	17	17	17	17	17	16	14	12	9	4	268

% Good Devices 50.5%% Correlation 74.5%

Table VI Correlation Summary

Wafer N21

Device Diode with Guard Ring

Test Breakdown < 50 volts

Device Evaluation Probe	Material Characteri- zation by X-ray	C O L U M N																				Catagory Total
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Passed	Good Material	3	4	1	7	7	11	10	11	11	10	12	10	9	9	6	7	3	0	0		131
Failed	Defects	3	4	4	1	0	0	0	0	1	2	2	3	3	3	6	4	2	5	3		46
Passed	Defects	1	1	0	0	0	0	0	0	0	0	0	0	0	0	3	3	5	4	1		18
Failed	Good Material	0	1	7	7	9	6	7	6	5	5	3	4	5	5	1	0	2	0	0		73
Column Total		7	10	12	15	16	17	17	17	17	17	17	17	17	17	16	14	12	9	4		268

% Good Devices 55.5%

% Correlation 66%

Wafer N22Table VII Correlation Summary  
Device Diode with Guard RingTest Breakdown < 50 volts

Device Evaluation Probe	Material Characteri- zation by X-ray	C O L U M N																				Category Total
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
Passed	Good Material	0	0	2	4	7	11	13	11	13	14	13	12	11	10	8	4	3	0	0		136
Failed	Defects	6	10	6	1	1	1	1	1	2	1	0	3	4	3	4	7	9	7	2		69
Passed	Defects	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2		5
Failed	Good Material	0	0	4	10	8	5	3	5	2	2	4	2	2	4	4	3	0	0	0		58
Column Total		7	10	12	15	16	17	17	17	17	17	17	17	17	17	16	14	12	9	4		268

% Good Devices 52.5%% Correlation 76.5%

#### IV SUMMARY OF APPLICATIONS AND RECENT IMPROVEMENTS

The continuously variable curvature elastic chuck shown in Figure 12 has replaced the earlier fixed curvature rigid chuck. The new chuck allows custom bending of each individual wafer in order to maximize the area that is imaged. The new chuck can accomodate all of the common cuts of all the common semiconductor materials; even those that are accidentally or deliberately cut off of one of the major crystallographic axes. Experiments have been conducted using tapered elastic membranes to obtain the optimum radial variation of stiffness for a broad variety of wafer sizes and thicknesses.

Exposure times have recently been reduced by 50% by placing thin mylar windows on each end of the scatter tube and flushing the tube with helium gas. The helium gas absorbs a negligible amount of the copper characteristic radiation while an equal length air path absorbs about one half of this radiation. The helium flush also gives a significant improvement to the image contrast since the harder continuous radiation (which contributes only to the image background) is transmitted equally well by either air or helium.

The drawing in Figure 13 shows a prototype x-ray image converter which has been used to demonstrate the feasibility of using real time TV system for low resolution x-ray topography as well as for rapid camera settings prior to conventional "hard copy" exposures. The x-rays enter through the black plastic (which blocks all visible light) and strike the phosphor coated glass plate. The phosphors convert the x-ray image into visible light. The evaporated aluminum coating serves to

# ELASTIC CHUCK

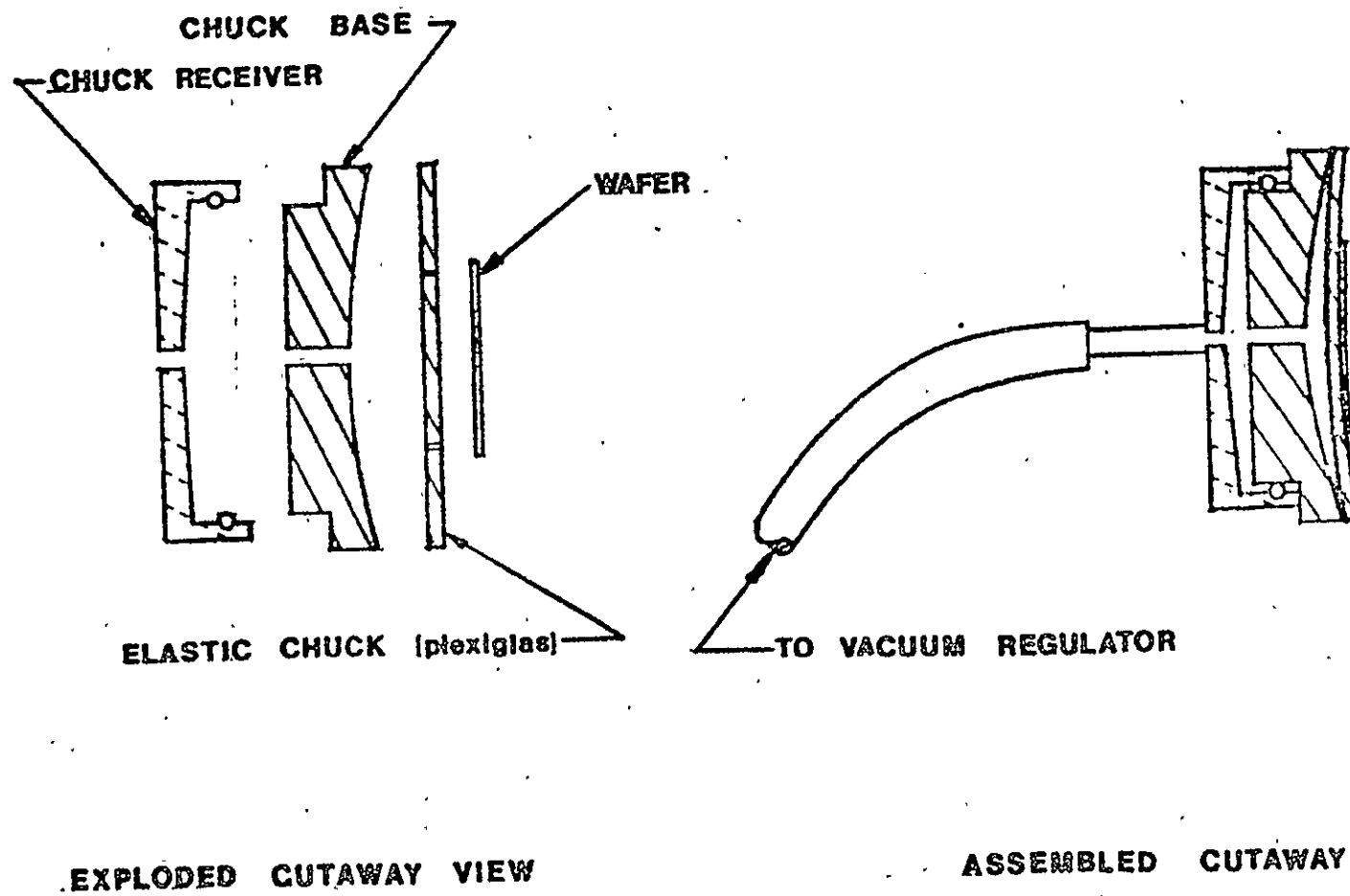
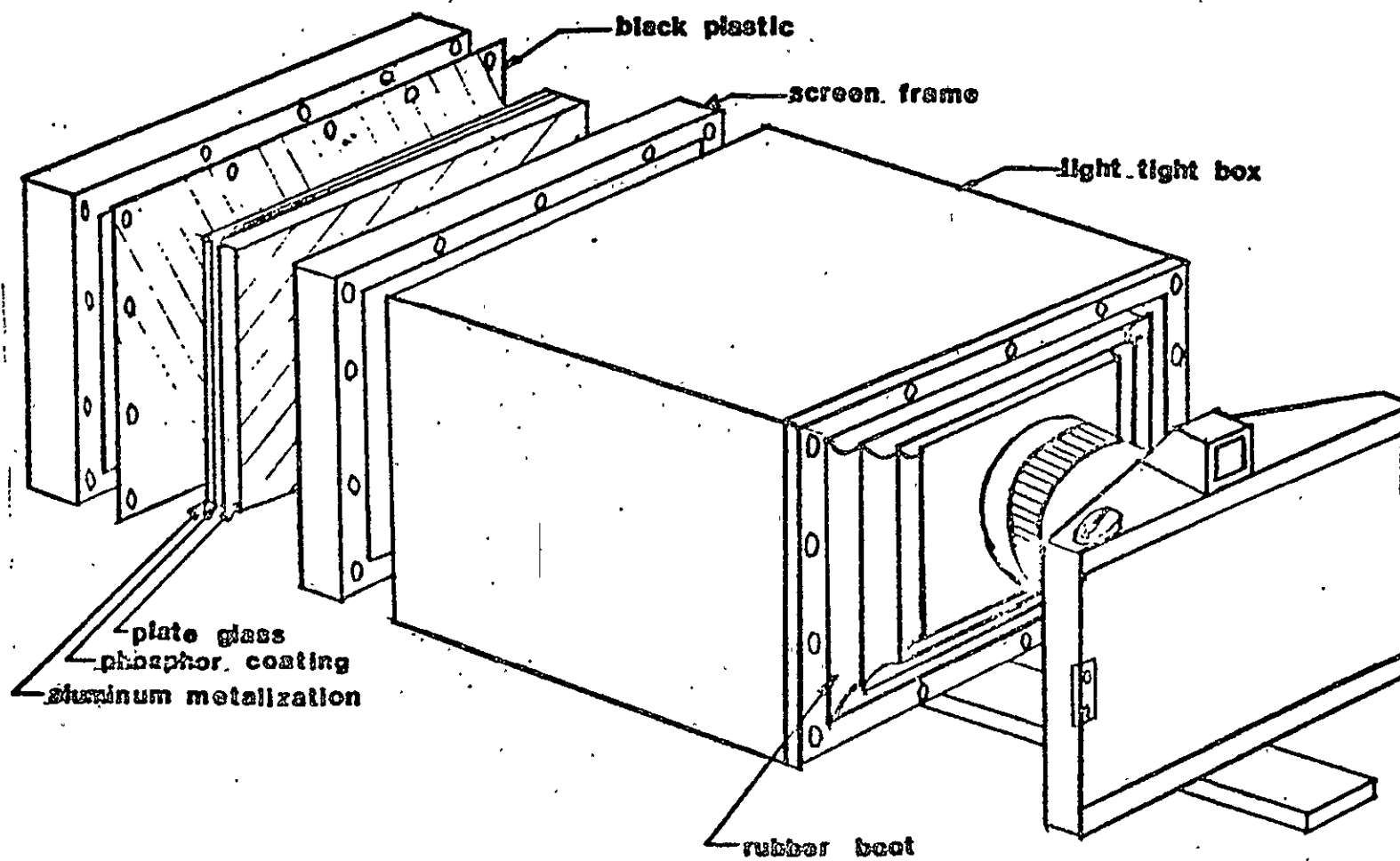


Figure 12



## **X-RAY IMAGE CONVERTER**

Figure 13

double the light output by reflecting the visible light back toward the camera. A 35 mm still camera was used for the demonstration. However, this will be replaced by a silicon intensified target low light level TV camera.

Figure 14 is a direct transmission radiograph of an inline package that was made with the image converter and 35 mm camera. Figure 15 is an x-ray topograph of a two inch silicon wafer made with this arrangement. The x-ray topograph has less resolution and contrast than the radiograph due to the fact that the phosphor coating currently being used is relatively insensitive to the copper characteristic radiation. Due to the diffraction process the characteristic radiation forms the entire image in the topograph whereas all x-ray wavelengths are used in forming the radiograph image. The relative insensitivity of the phosphor coating to the characteristic radiation considerably degrades the topograph image since the background (noise) is anonymously high and the desired diffracted image is anonymously low. We are currently searching for more favorable phosphors as well as experimenting with additional coatings in order to reverse this unfavorable sensitivity ratio.

The problem of finding a phosphor coating which resonates at a particular wavelength is unique since all previous applications of x-ray fluoroscopy involve a continuous distribution of energies (usually much higher energies). Since so little previous work has been done in this area, rapid and significant improvements in the phosphor coatings for our particular application are probable.

Even without improved phosphor coatings the topograph in Figure 15 demonstrates the feasibility of using the TV system for initial alignment

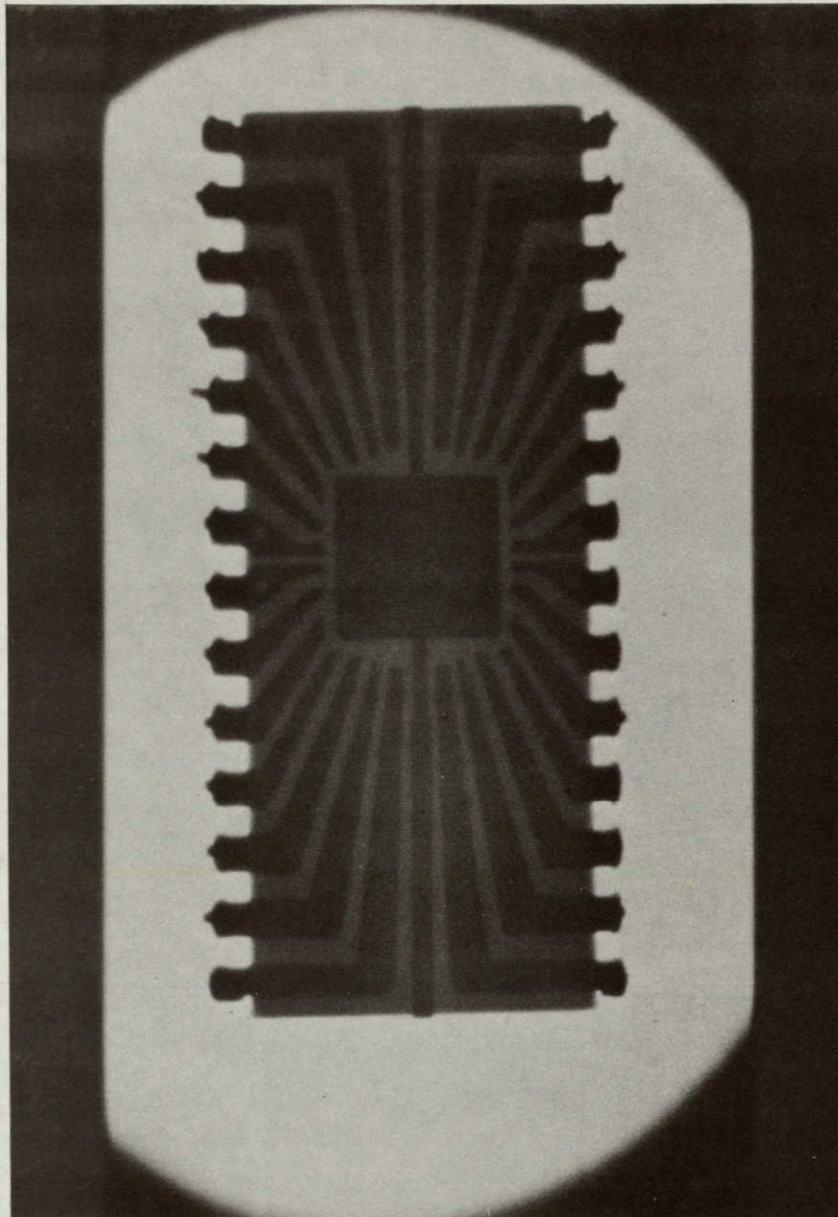


Figure 14 X-ray radiograph of an inline package. This photograph was made with the TV simulator using the 35 mm still camera and panatimic X film.



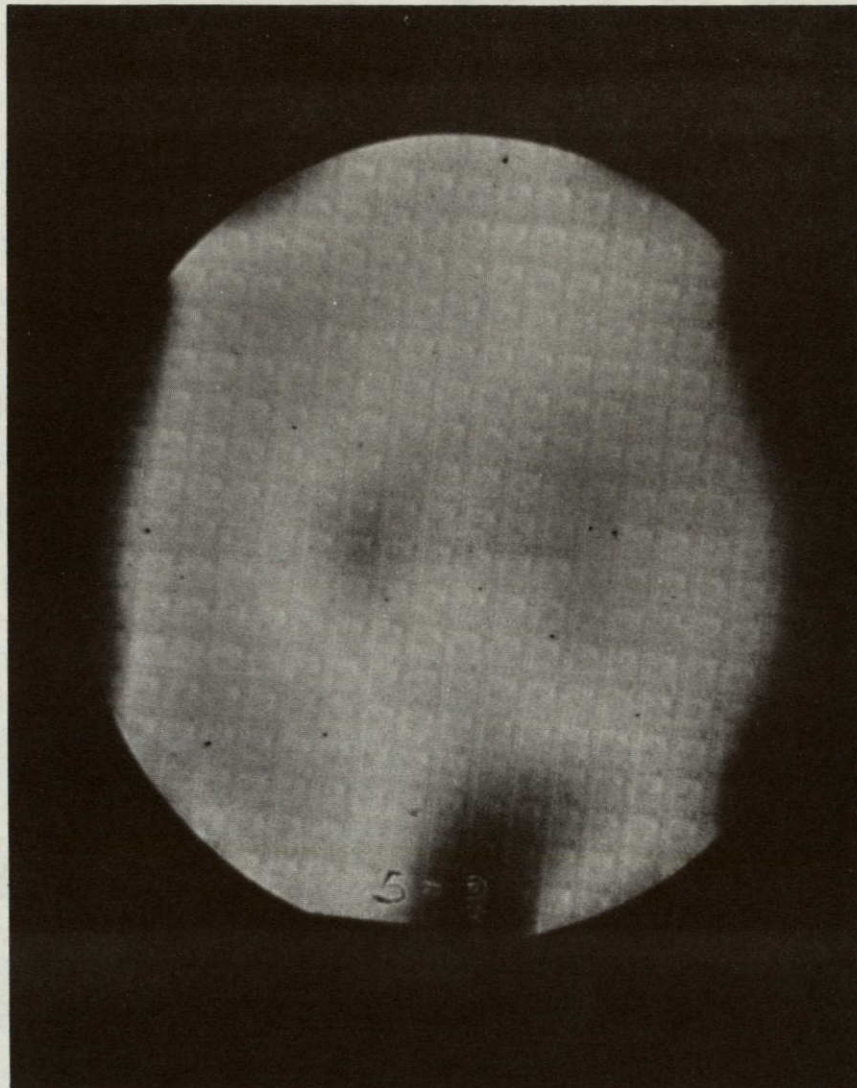


Figure 15 X-Ray topograph of a two inch silicon wafer. This topograph was made with the TV simulator and 35 mm camera. The image contrast is poor due to the relative insensitivity of the phosphors which are currently being used to copper radiation.



and detection of gross damage. In round numbers the TV system will cost about \$5K to \$8K. This cost is partially offset by the fact that it will replace the \$2K to \$3K worth of detection electronics which is ordinarily used for initial alignment. This price differential is a small price to pay for the increase in overall performance it will give as well as its potential application in other areas such as real time radiography, crystal orientation, etc.

We have worked with several different companies to find ways to use the x-ray camera to solve processing and wafer screening problems. Figure 16 is an x-ray topograph of a two inch silicon wafer found to have severe resistivity striations in the starting material. Figure 17 is a 70X enlargement of a portion of an x-ray topograph of a silicon wafer. Individual circuits from this wafer are being selected for packaging and reliability testing. Some circuits with and some without slip defects will be used in this test.

Figure 18 is an 18X enlargement of an x-ray topograph of a silicon-on-sapphire wafer after processing and probe. Figure 19 is a 70X enlargement of this same topograph. These topographs show a considerable amount of material defects. And Figure 20 is a 70X enlargement of an x-ray topograph of a GaAs slice after zinc diffusion. The zinc diffusion is found to cause considerably more lattice damage than an otherwise identical thermal cycle.

Figure 21 is an x-ray topograph of a silicon wafer used in an experiment to explore the feasibility of using x-ray diffraction as a means of measuring the sheet resistivity obtained during a diffusion step.



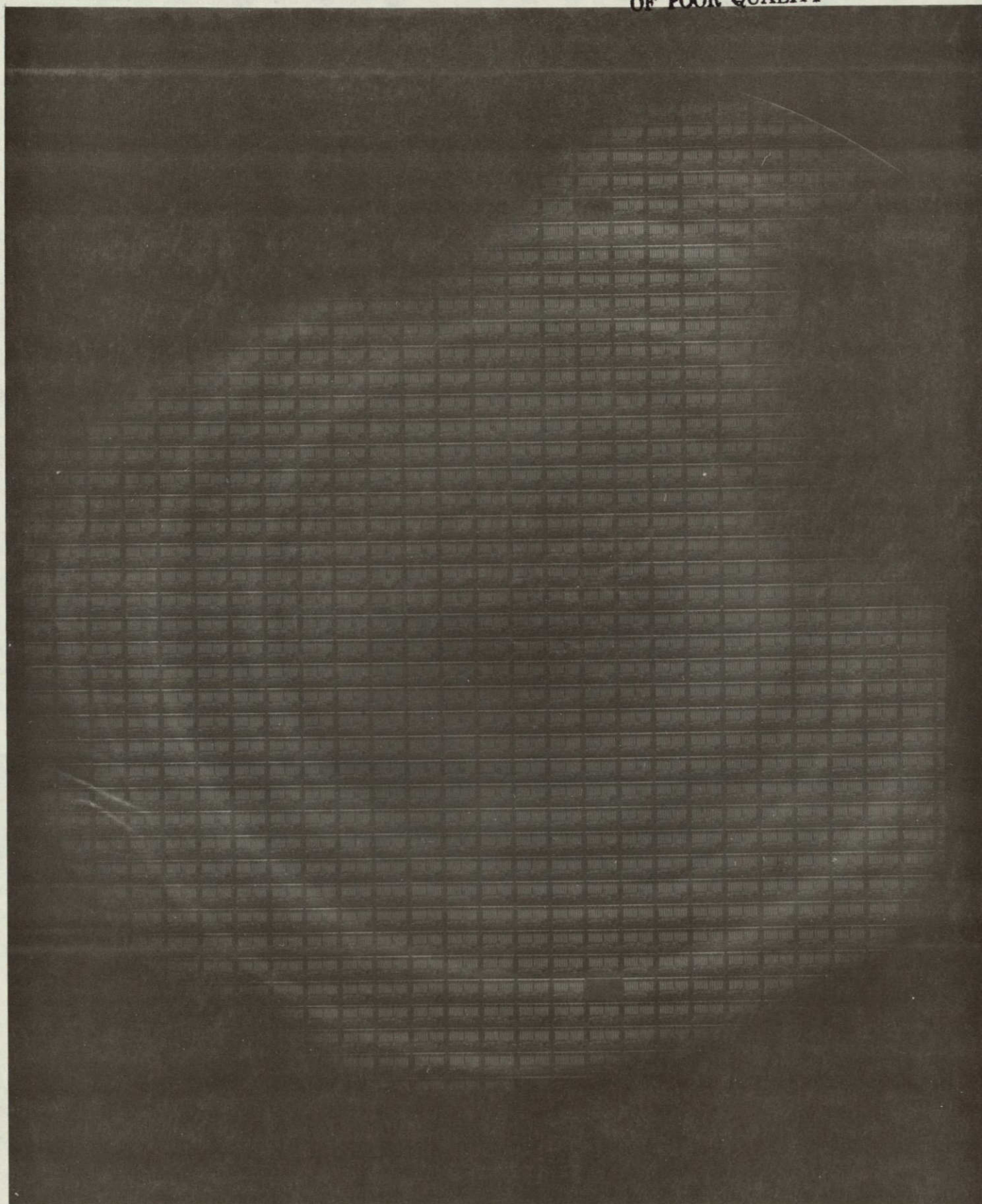


Figure 16 Current production two inch silicon wafer.



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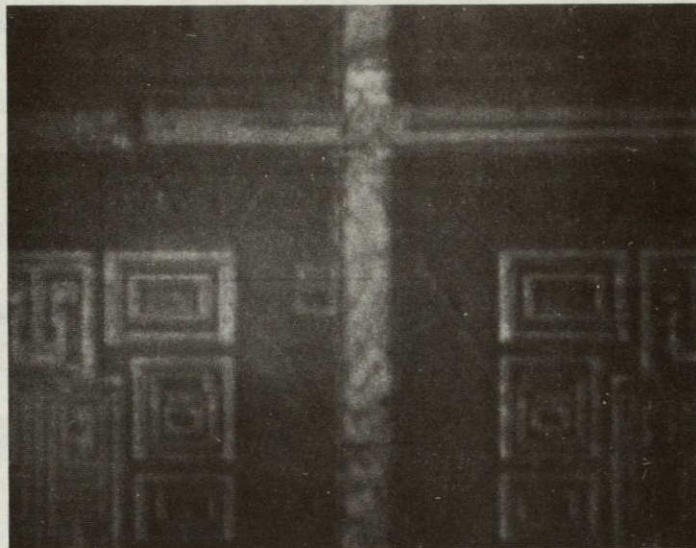


Figure 17 70X enlargement of an x-ray topograph of a current production silicon wafer. Circuits from this wafer are being selected on the basis of defects shown in the original topograph for reliability testing.



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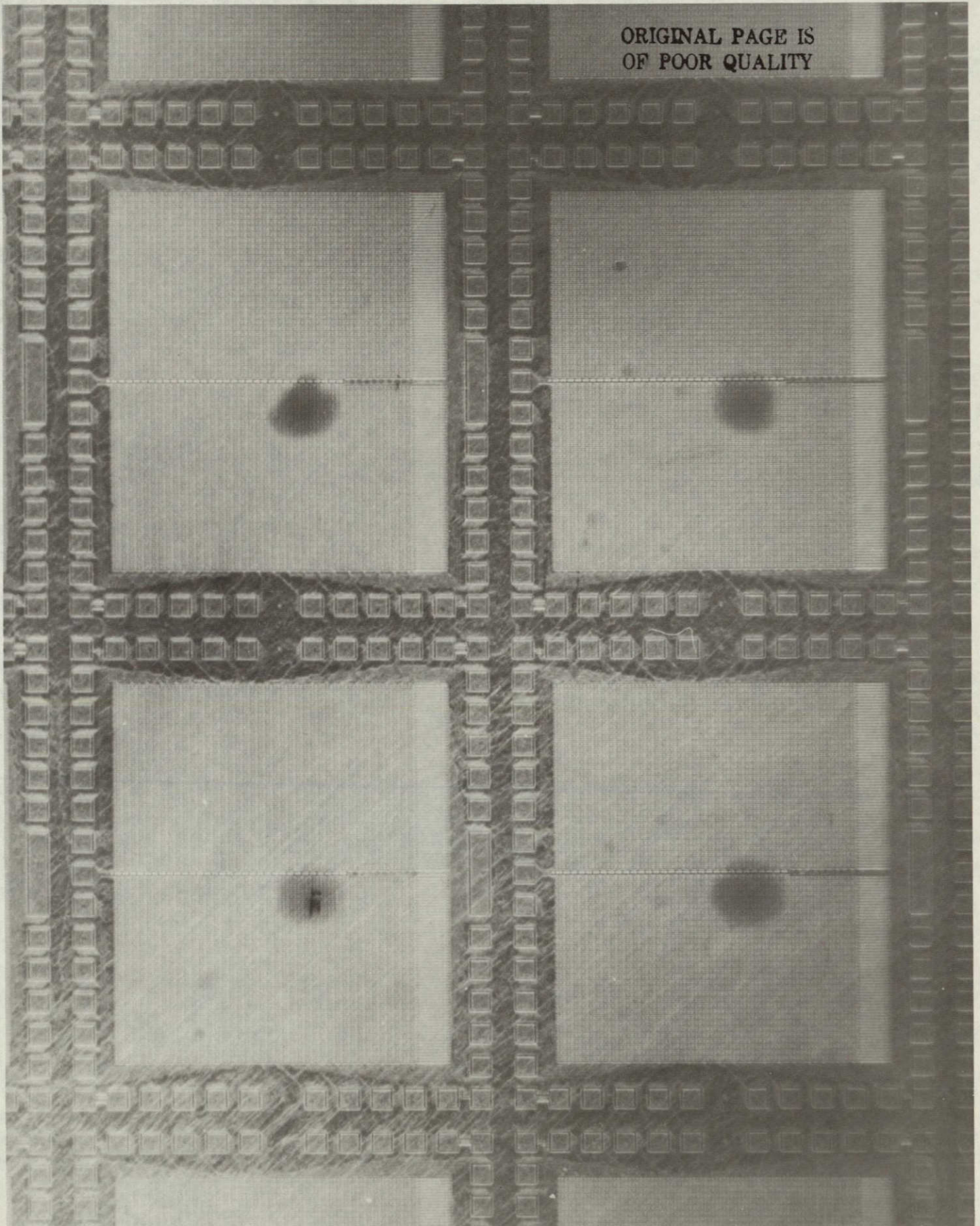


Figure 18 18X enlargement of a silicon-on-sapphire x-ray topograph.



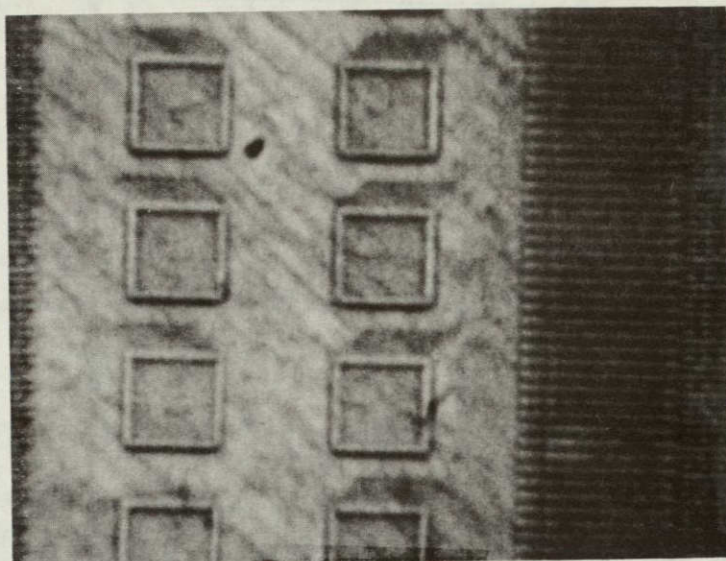


Figure 19 70X enlargement of an SOS topograph.

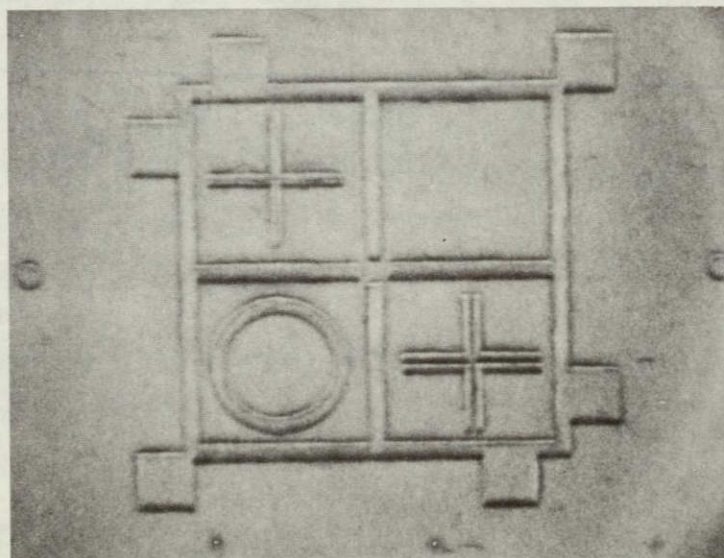


Figure 20 70X enlargement of GaAs topograph



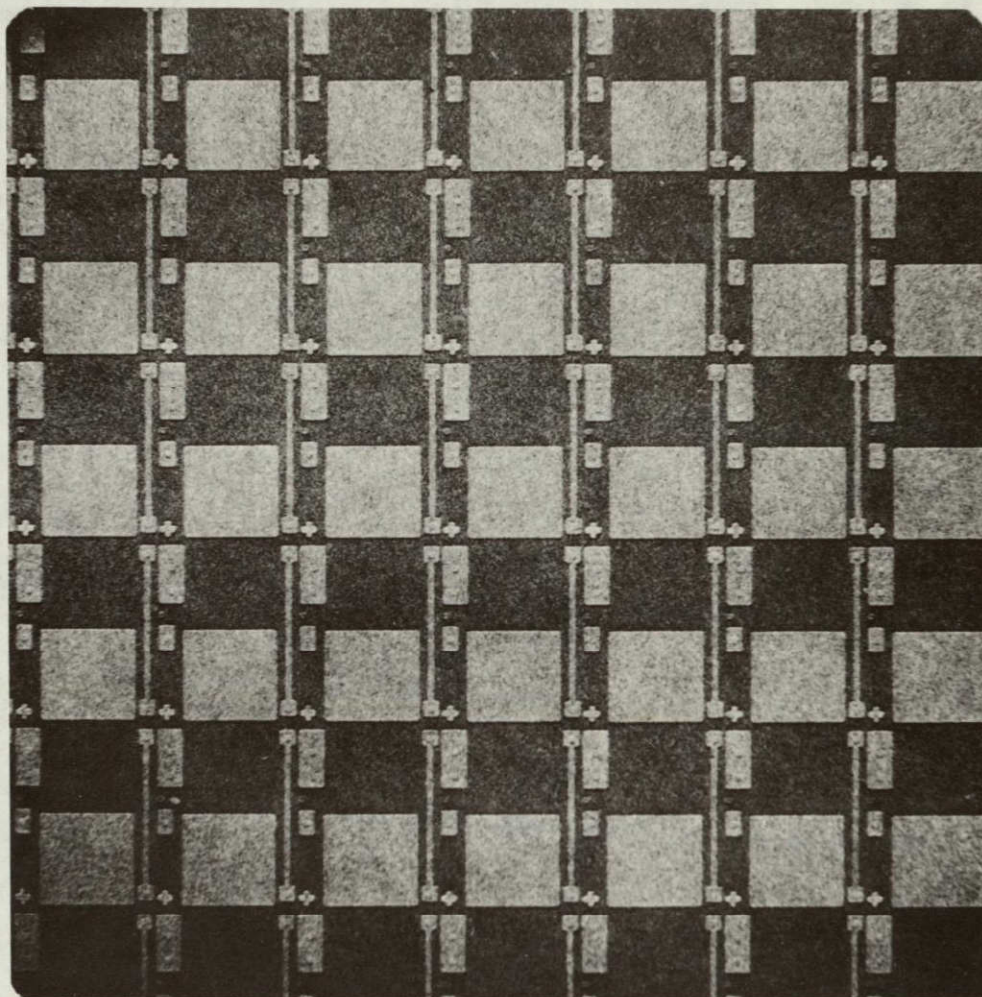


Figure 21 4.7X enlargement of an x-ray topograph of a silicon wafer. This test pattern is being used to investigate the feasibility of using x-ray diffraction to measure the uniformity of the sheet resistivity obtained during a typical diffusion step.

The large white squares are 100 x 100 mils and received a diffusion (as did all other areas of similar shading). The enlargement is a positive which means the light areas are diffracting more strongly than the dark. One current graduate student has adopted as a thesis topic the study of the variation of the x-ray diffracting power with doping species and density, junction depth, and x-ray incidence angle.

A careful examination of the topograph in Figure 21 will show that the aluminum contacts are visible in the diodes and resistors. Also a considerable amount of damage is visible. This damage was in the original starting material.

To summarize, what has been given here is a very small sample of the total amount of work which has been done in the refinement and application of the bent wafer x-ray topographic camera. Each of the areas touched here underline the broad potential of the camera in solving a variety of todays processing problems.



## APPENDIX

In a research contract such as NAS8-26379 an additional measure of its success are the number of graduate students it supported and the work they did as well as the number of technical papers accepted for publication and presentation.

The lists of the students, their research topics and relevant publications and presentations are given below:

### Graduate Students

Surinder Goklaney, Ph.D.

Fouad Raphael, M.S.

Lynn Reed, M.S.

K. C. Patel, M.S.

Taira Nishizono, M.S.

Andrew Huang, M.S.

Wayne Bibeau, M.S.

Agnisarman Namboodiri, Ph.D.

### Thesis/Dissertation Topic

"The Effects of Dislocations on the Electrical Properties of Thermally Grown Silicon Dioxide Films"

"The Influence of Dislocations on the Electrical Characteristics of P-Channel Insulated Gate Field Effect Transistors"

"The Effectiveness of Stress Relief Etching for Improving Bipolar Device Characteristics"

"Effects of Interfacial Oxide Layers on the Current-Voltage Characteristics of Al-Si Contacts"

"A Study of the Combined Influence of Temperature and Material Defects on Semiconductor Device Performance"

"Correlation Study of Boron Diffusion Sources with the Material and Electrical Characteristics of Semiconductor Junctions"

Current Student

Current Student

## PUBLICATIONS

<u>Title</u>	<u>Journal</u>
"A High Speed X-ray Topographic Camera for Semiconductor Wafer Evaluation"	Journal of the Electrochemical Society, Vol. 123, No 1, January 1976.
"The Effect of a Prior Sirtl Etch on Subsequent Thermally Induced Processing Damage in Silicon Wafers"	Journal of the Electrochemical Society, vol. 123, No 3 March 1976.
"Investigation of Dislocation Creation in Silicon After Thermal Oxidation and Phosphorous Diffusion"	Journal of the Institution of Engineers, India, 1974.
"Interlay Shear Stress at the Silicon-Silicon Dioxide Interface"	Indian Journal of Technology, 1974.
"The Effect of Dislocations on Capacitance vs. Voltage Characteristics of MOS Capacitors"	IEEE-IERE Proceedings, India 1974.
"Defect Analysis and Yield Degradation of Integrated Circuits"	Journal of Solid State Circuits Vol. SC-9, no 3, June 1974.
"The Performance of Ion Implanted and Diffused MOSFETS in Plastically Deformed Silicon"	TEES Technical Bulletin #74-2 April 1974.
"Use of Sirtl Etch for Silicon Slice Evaluation"	Journal of the Electrochemical Society, vol. 120, no. 4, April 1973.
"Influence of Carrier Curvature on Thermally Induced Imperfections in Silicon"	TEES Technical Bulletin #72-1 December 1972.
"Process-Induced Dislocation Reductions in Silicon By Chemical Etching Techniques"	Electronics and Dielectrics General Sessions of the Electrochemical Society, May 1973.
"The Role of Defects in Semiconductor Device Reliability"	SWIEECO, 1972.
"A Thermal Cycling System for Semiconductor Device Processing"	SWIEECO, 1971.
"Strain Generated Surface Patterns in Silicon"	SWIEECO, 1970.

## LECTURES

<u>Title</u>	<u>Conference</u>
"Process-Induced Dislocation Reductions in Silicon by Chemical Etching Techniques"	Electronics and Dielectrics General Sessions of the Electrochemical Society May 1973
"The Role of Defects in Semiconductor Device Reliability"	SWIEECO, 1972
"A Thermal Cycling System for Semiconductor Device Processing"	SWIEECO, 1971
"Strain Generated Surface Patterns In Silicon"	SWIEECO, 1970